AMENDMENTS TO THE CLAIMS:

Please amend the claims as follows:

1. (Currently amended) A semiconductor memory comprising:

a plurality of word lines;

a plurality of memory cells provided on a semiconductor substrate, each of the memory cells including a MISFET including a first doped layer, a second doped layer and a gate electrode;

wherein for first and second memory cells of the plurality of memory cells that are adjacent to each other ~~and arranged in the direction in which the bit lines extend~~:

a first dummy gate electrode connected to a first power supply is provided between a first doped layer of a first MISFET included in the first memory cell and a first doped layer of a second MISFET included in the second memory cell, and

the first doped layer of the first MISFET, the first doped layer of the second MISFET and the first dummy gate electrode together constitute a first dummy MISFET which is held OFF during operation.

2. (Currently amended) The semiconductor memory of claim 1, wherein each of the plurality of memory cells is constituted by a MISFET, and

data is recorded in accordance with whether or not the first doped ~~layers~~ layer of the ~~MISFETs~~ MISFET constituting the respective memory ~~cells are~~ cell is connected to the bit ~~lines~~ line.

3. (Original) The semiconductor memory of claim 1, wherein the MISFETs included in the plurality of memory cells and the first dummy MISFET are of an n-channel type, and the first power supply is a ground line.

4. (Original) The semiconductor memory of claim 1, wherein the MISFETs included in the plurality of memory cells and the first dummy MISFET are of an n-channel type, and the first power supply is a power supply for supplying a negative voltage.

5. (Original) The semiconductor memory of claim 1, wherein a threshold value of the first dummy MISFET has an absolute value larger than that of a threshold value of each of the MISFETs included in the plurality of memory cells.

6. (Original) The semiconductor memory of claim 1, wherein the first dummy gate electrode has a gate length larger than that of a gate electrode of each of the MISFETs included in the plurality of memory cells.

7. (Original) The semiconductor memory of claim 1, wherein first and second gate insulating films are provided between the gate electrodes of the MISFETs included in the plurality of memory cells and the semiconductor substrate and between the first dummy gate electrode and

the semiconductor substrate, respectively, and the second gate insulating film has a thickness larger than that of the first gate insulating film.

8. (Original) The semiconductor memory of claim 1, wherein among the MISFETs included in the plurality of memory cells, gate electrodes of those MISFETs arranged in one row in the direction in which the word lines extend are also part of a common gate line, and

the gate line has a branch extending toward a region interposed between first doped layers of those MISFETs adjacent to each other and arranged in the direction in which the word lines extend, among the MISFETs included in the plurality of memory cells.

9. (Original) The semiconductor memory of claim 1, wherein the semiconductor substrate is a partially depleted SOI substrate including:

a buried insulating film; and

a semiconductor layer provided on the buried insulating film and including first and second doped layers, and

a negative voltage is applied to the semiconductor layer.

10. (Original) The semiconductor memory of claim 1, further comprising

a word line driver including first driver MISFETs of an n-channel type and second driver MISFETs of a p-channel type and used for setting potentials on the plurality of word lines, the first and second driver MISFETs being connected to the plurality of word lines,

wherein a second dummy MISFET including a second dummy gate electrode and held OFF during operation is further provided between two of the first driver MISFETs connected to those word lines adjacent to each other among the plurality of word lines.

11. (Original) The semiconductor memory of claim 10, wherein each of the first and second dummy MISFETs is plural in number, and those first and second dummy MISFETs arranged in one row in the direction in which the word lines extend respectively have first and second dummy gate electrodes which are also part of a common dummy gate line.

12. (Original) The semiconductor memory of claim 10, wherein the MISFETs included in the plurality of memory cells and the first dummy MISFET are of an n-channel type, second doped layers of the MISFETs included in the plurality of memory cells and second doped layers of the first driver MISFETs are connected to the first power supply, and the first power supply is a power supply for supplying a negative voltage.

13. (Original) A semiconductor integrated circuit comprising:

a semiconductor memory comprising a plurality of word lines, a plurality of bit lines crossing the plurality of word lines and a plurality of first memory cells, the first memory cells

being provided on a first semiconductor substrate and each including a MISFET including a first doped layer, a second doped layer and a gate electrode;

a circuit block including a MISFET provided on a semiconductor substrate and a logic circuit; and

a power supply circuit for supplying a fixed potential to at least part of the first semiconductor substrate,

wherein for third and fourth memory cells of the plurality of first memory cells that are adjacent to each other and arranged in the direction in which the bit lines extend, a dummy MISFET which includes a dummy gate electrode connected to a first power supply, a third doped layer and a fourth doped layer and is held OFF during operation is provided between a first doped layer of a first MISFET included in the third memory cell and a first doped layer of a second MISFET included in the fourth memory cell.

14. (Original) The semiconductor integrated circuit of claim 13, wherein the circuit block further includes at least one circuit selected from the group consisting of a DRAM, an SRAM and a nonvolatile memory.

15. (Original) The semiconductor integrated circuit of claim 13, wherein the MISFETs included in the plurality of memory cells and the dummy MISFET are of an n-channel type, and the first power supply is a power supply for supplying a negative voltage.

16. (Original) The semiconductor integrated circuit of claim 15, wherein the power supply circuit supplies a negative voltage to part of the first semiconductor substrate and part of the semiconductor substrate in the circuit block.

17. (Original) The semiconductor integrated circuit of claim 16, wherein a switch for selecting either one of an output voltage from the power supply circuit or a ground voltage to be

supplied to the logic circuit is further provided between the power supply circuit and the logic circuit.